ABSTRACT OF THE DISCLOSURE

A feedback latch circuit includes a first logic OR gate for performing a logic OR operation upon a clock input signal and a latch output, a first logic AND gate for performing a logic AND operation upon output of the first logic OR gate and a data input signal, a second logic AND gate for performing a logic AND operation upon a complementary clock input signal and the latch output, and a second logic OR gate for performing a logic OR operation upon outputs of the first and second logic AND gates to result in the latch output that is provided to the first logic OR gate and the second logic AND gate. The complementary clock input signal received by the second logic AND gate complements the clock input signal received by the first logic OR gate.